UNITED STATES PATENT APPLICATION

LANTHANIDE OXIDE / HAFNIUM OXIDE DIELECTRICS

INVENTORS

Kie Y. Ahn

of Chappaqua, NY

and

Leonard Forbes

of Corvallis, OR

LANTHANIDE OXIDE / HAFNIUM OXIDE DIELECTRICS

Cross Reference To Related Applications

This application is related to the co-filed and commonly assigned U.S. patent
5 application, attorney docket number 303.101US1, Serial No. _____, entitled
"Lanthanide Oxide / Hafnium Oxide Dielectric Layers," which is hereby
incorporated by reference in its entirety.

Technical Field

10 This application relates generally to semiconductor devices and device
fabrication and, more particularly, to dielectric layers and their method of
fabrication.

Background

15 The semiconductor device industry has a market driven need to improve
speed performance, improve its low static (off-state) power requirements, and adapt
to a wide range of power supply and output voltage requirements for its silicon
based microelectronic products. In particular, there is continuous pressure to reduce
the size of devices such as transistors. The ultimate goal is to fabricate increasingly
20 smaller and more reliable integrated circuits (ICs) for use in products such as
processor chips, mobile telephones, and memory devices such as dynamic random
access memories (DRAMs).

Currently, the semiconductor industry relies on the ability to reduce or scale
the dimensions of its basic devices, primarily, the silicon based metal-oxide-
25 semiconductor field effect transistor (MOSFET). A common configuration of such
a transistor is shown in Figure 1. While the following discussion uses Figure 1 to
illustrate a transistor from the prior art, one skilled in the art will recognize that the
present invention could be incorporated into the transistor shown in Figure 1 to form
a transistor according to the present invention. A transistor 100 is fabricated in a
30 substrate 110 that is typically silicon. Transistor 100 has a source region 120 and a
drain region 130. A body region 132 is located between source region 120 and

drain region 130, where body region 132 defines a channel of the transistor with a channel length 134. A gate dielectric 140 is located on body region 132 with a gate 150 located over gate dielectric 140. Gate dielectric 140 is typically an oxide, and is commonly referred to as a gate oxide. Gate 150 may be fabricated from
5   polycrystalline silicon (polysilicon), or other conducting materials such as metal may be used.

In fabricating transistors to be smaller in size and reliably operate on lower power supplies, one design criteria is gate dielectric 140. The mainstay for forming the gate dielectric has been silicon dioxide, SiO_2. A thermally grown amorphous
10   SiO_2 layer provides an electrically and thermodynamically stable material, where the interface of the SiO_2 layer with underlying Si provides a high quality interface as well as superior electrical isolation properties. However, increased scaling and other requirements in microelectronic devices have created the need to use other dielectric materials as gate dielectrics.
15

Summary

The abovementioned problems are addressed by the present invention and will be understood by reading and studying the following specification. An embodiment for a method for forming a dielectric layer containing a hafnium oxide
20   and a lanthanide oxide includes forming a layer of hafnium oxide by chemical vapor deposition and forming a layer of lanthanide oxide by electron beam evaporation. The layer of hafnium oxide is adjacent to and in contact with the layer of lanthanide oxide. In an embodiment, a dielectric layer includes a hafnium oxide / lanthanide oxide nanolaminate having a chemical vapor deposited hafnium oxide layer and an
25   electronic beam evaporated lanthanide oxide layer.

Dielectric layers containing a chemical vapor deposited hafnium oxide layer and an electronic beam evaporated lanthanide oxide layer have a larger dielectric constant than silicon dioxide. Such dielectric layers provide a significantly thinner equivalent oxide thickness compared with a silicon oxide layer having the same
30   physical thickness. Alternately, such dielectric layers provide a significantly thicker physical thickness than a silicon oxide layer having the same equivalent oxide

thickness. Embodiments include structures for capacitors, transistors, memory devices, and electronic systems with dielectric layers containing a chemical vapor deposited hafnium oxide layer and an electronic beam evaporated lanthanide oxide layer, and methods for forming such structures.

5   These and other aspects, embodiments, advantages, and features will become apparent from the following description and the referenced drawings.

Brief Description of the Drawings

Figure 1 shows a configuration of a transistor having a gate dielectric

10 containing a chemical vapor deposited hafnium oxide layer and an electronic beam evaporated lanthanide oxide layer, according to various embodiments of the present invention.

Figure 2 depicts a block diagram for a chemical vapor deposition system for processing a layer of hafnium oxide for a dielectric layer containing a hafnium

15 oxide and a lanthanide oxide, according to various embodiments of the present invention.

Figure 3 depicts an electron beam evaporation system for processing a layer of lanthanide oxide for a dielectric layer containing a hafnium oxide and a lanthanide oxide, according to various embodiments of the present invention.

20 Figure 4 illustrates a flow diagram of elements for an embodiment of a method to process a dielectric layer containing a chemical vapor deposited hafnium oxide layer and an electronic beam evaporated lanthanide oxide layer, according to the present invention.

Figure 5 illustrates a flow diagram of elements for an embodiment of a

25 method to process a dielectric layer containing a chemical vapor deposited hafnium oxide layer and an electronic beam evaporated lanthanide oxide layer, according to the present invention.

Figure 6 depicts an embodiment of a dielectric layer including a nanolaminate of hafnium oxide and lanthanide oxide, according to the present

30 invention.

Figure 7 shows an embodiment of a configuration of a transistor having a dielectric layer containing a chemical vapor deposited hafnium oxide layer and an electronic beam evaporated lanthanide oxide layer, according to the present invention.

5   Figure 8 shows an embodiment of a configuration of a capacitor having a dielectric layer containing a chemical vapor deposited hafnium oxide layer and an electronic beam evaporated lanthanide oxide layer, according to the present invention.

Figure 9 is a simplified block diagram for an embodiment of a memory
10   device with a dielectric layer containing a chemical vapor deposited hafnium oxide layer and an electronic beam evaporated lanthanide oxide layer, according to the present invention.

Figure 10 illustrates a block diagram for an embodiment of an electronic system having devices with a dielectric layer containing a chemical vapor deposited
15   hafnium oxide layer and an electronic beam evaporated lanthanide oxide layer, according to the present invention.

Detailed Description

The following detailed description refers to the accompanying drawings that
20   show, by way of illustration, specific aspects and embodiments in which the present invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the present invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The various embodiments
25   disclosed herein are not necessarily mutually exclusive, as some disclosed embodiments can be combined with one or more other disclosed embodiments to form new embodiments.

The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form an integrated circuit (IC).
30   The term substrate is understood to include semiconductor wafers. The term substrate is also used to refer to semiconductor structures during processing, and

may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art.

5   The term "horizontal" as used in this application is defined as a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. The term "vertical" refers to a direction perpendicular to the horizontal as defined above. Prepositions, such as "on", "side" (as in "sidewall"), "higher", "lower", "over" and "under" are defined with respect to

10   the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the orientation of the wafer or substrate. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

15   In various embodiments, a dielectric layer includes a hafnium oxide layer and a lanthanide oxide layer, where the hafnium oxide layer is formed by chemical vapor deposition (CVD) and the lanthanide oxide layer is formed by electron beam evaporation. The lanthanide oxide can be selected from Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, and Dy_2O_3. In an embodiment, a dielectric layer includes a hafnium oxide /

20   lanthanide oxide nanolaminate.

          The term "nanolaminate" means a composite film of ultra thin layers of two or more materials in a layered stack, where the layers are alternating layers of materials of the composite film. Typically, each layer in a nanolaminate has a thickness of an order of magnitude in the nanometer range, up to several tens of

25   nanometers. Further, each individual material layer of the nanolaminate can have a thickness as low as a monolayer of the material. A nanolaminate of hafnium oxide and a lanthanide oxide includes at least one thin layer of hafnium oxide, and one thin layer of the lanthanide oxide, which can be written as a nanolaminate of hafnium oxide / lanthanide oxide. Further, a hafnium oxide / lanthanide oxide

30   nanolaminate is not limited to alternating one lanthanide layer after a hafnium oxide layer, but can include multiple thin layers of a lanthanide oxide alternating with

multiple thin layers of hafnium oxide. Further, the number of thin layers of lanthanide oxide and the number of thin layers of hafnium oxide can vary independently within a nanolaminate structure. Additionally, a hafnium oxide / lanthanide oxide nanolaminate can include layers of different lanthanide oxides,

5   where each layer is independently selected from Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, and Dy_2O_3. A dielectric layer containing alternating layers of a lanthanide oxide and a hafnium oxide has an effective dielectric constant related to the series combination of the layers of lanthanide oxide and hafnium oxide, which depends on the relative thicknesses of the lanthanide oxide layers and the hafnium oxide layers. Thus, a

10   dielectric containing a hafnium oxide / lanthanide oxide nanolaminate can be engineered to effectively provide a selected dielectric constant.

A gate dielectric 140 of Figure 1, when operating in a transistor, has both a physical gate dielectric thickness and an equivalent oxide thickness (t_{eq}). The equivalent oxide thickness quantifies the electrical properties, such as capacitance,

15   of a gate dielectric 140 in terms of a representative physical thickness. The equivalent oxide thickness, t_{eq}, is defined as the thickness of a theoretical SiO_2 layer that would have the same capacitance density as a given dielectric, ignoring leakage current and reliability considerations.

A SiO_2 layer of thickness, t, deposited on a Si surface as a gate dielectric

20   will have a t_{eq} larger than its thickness, t. This t_{eq} results from the capacitance in the surface channel on which the SiO_2 is deposited due to the formation of a depletion/inversion region. This depletion/inversion region may result in t_{eq} being from 3 to 6 Angstroms (Å) larger than the SiO_2 thickness, t. Thus, with the semiconductor industry driving to scale the gate dielectric equivalent oxide

25   thickness to under 10 Å, the physical thickness for a SiO_2 layer used for a gate dielectric would be need to be approximately 4 to 7 Å.

Additional characteristics for a SiO_2 layer depend on the gate electrode used in conjunction with the SiO_2 gate dielectric. Using a conventional polysilicon gate results in an additional increase in t_{eq} for the SiO_2 layer. This additional thickness

30   could be eliminated by using a metal gate electrode, though metal gates are not currently used in typical complementary metal-oxide-semiconductor field effect

transistor (CMOS) technology. Thus, future devices would be designed towards a physical SiO_2 gate dielectric layer of about 5 Å or less. Such a small thickness for a SiO_2 oxide layer creates additional problems.

Silicon dioxide is used as a gate dielectric, in part, due to its electrical isolation properties in a SiO_2 - Si based structure. This electrical isolation is due to the relatively large bandgap of SiO_2 (8.9 eV) making it a good insulator from electrical conduction. Signification reductions in its bandgap would eliminate it as a material for a gate dielectric. As the thickness of a SiO_2 layer decreases, the number of atomic layers, or monolayers of the SiO_2 decreases. At a certain thickness, the number of monolayers will be sufficiently small that the SiO_2 layer will not have a complete arrangement of atoms as in a larger or bulk layer. As a result of incomplete formation relative to a bulk structure, a thin SiO_2 layer of only one or two monolayers will not form a full bandgap. The lack of a full bandgap in a SiO_2 gate dielectric could cause an effective short between an underlying Si channel and an overlying polysilicon gate. This undesirable property sets a limit on the physical thickness to which a SiO_2 layer may be scaled. The minimum thickness due to this monolayer effect is thought to be about 7-8 Å. Therefore, for future devices to have a t_{eq} less than about 10 Å, dielectrics other than SiO_2 need to be considered for use as a gate dielectric.

For a typical dielectric layer used as a gate dielectric, the capacitance is determined as one for a parallel plate capacitance: $C = \kappa\epsilon_0 A/ t$, where κ is the dielectric constant, ϵ_0 is the permittivity of free space, A is the area of the capacitor, and t is the thickness of the dielectric. The thickness, t, of a material is related to its t_{eq} for a given capacitance, with SiO_2 having a dielectric constant $\kappa_{ox} = 3.9$, as

$$t = (\kappa/\kappa_{ox}) t_{eq} = (\kappa/3.9) t_{eq}.$$

Thus, materials with a dielectric constant greater than that of SiO_2, 3.9, will have a physical thickness that may be considerably larger than a desired t_{eq}, while providing the desired equivalent oxide thickness. For example, an alternate dielectric material with a dielectric constant of 10 could have a thickness of about 25.6 Å to provide a t_{eq} of 10 Å, not including any depletion/inversion layer effects. Thus, a reduced t_{eq} for transistors may be realized by using dielectric materials with

higher dielectric constants than SiO_2. The thinner t_{eq} for lower transistor operating voltages and smaller transistor dimensions may be realized by a significant number of materials, but additional fabricating characteristics makes determining a suitable replacement for SiO_2 difficult.

5   The current view for the microelectronics industry is still for Si based devices. Thus, the gate dielectric employed will grow on a silicon substrate or silicon layer, which places significant restraints on the substitute dielectric material. During the formation of the dielectric on the silicon layer, there exists the possibility that a small layer of SiO_2 could be formed in addition to the desired dielectric. The

10   result would effectively be a dielectric layer consisting of two sublayers in parallel with each other and the silicon layer on which the dielectric is formed. In such a case, the resulting capacitance would be that of two dielectrics in series. As a result, the t_{eq} of the dielectric layer would be the sum of the SiO_2 thickness and a multiplicative factor of the thickness of the dielectric being formed, written as

15    $$t_{eq} = t_{SiO_2} + (\kappa_{ox} / \kappa)t.$$
Thus, if a SiO_2 layer is formed in the process, the t_{eq} is again limited by a SiO_2 layer. Thus, use of an ultra-thin silicon dioxide interface layer should be limited to significantly less than ten angstroms. In the event that a barrier layer is formed between the silicon layer and the desired dielectric in which the barrier layer

20   prevents the formation of a SiO_2 layer, the t_{eq} would be limited by the layer with the lowest dielectric constant. However, whether a single dielectric layer with a high dielectric constant or a barrier layer with a higher dielectric constant than SiO_2 is employed, the layer interfacing with the silicon layer must provide a high quality interface to maintain a high channel carrier mobility.

25   One of the advantages for using SiO_2 as a gate dielectric has been that the formation of the SiO_2 layer results in an amorphous gate dielectric. Having an amorphous structure for a gate dielectric is advantageous because grain boundaries in polycrystalline gate dielectrics provide high leakage paths. Additionally, grain size and orientation changes throughout a polycrystalline gate dielectric may cause

30   variations in the layer's dielectric constant. Many materials having a high dielectric constant relative to SiO_2 also have a disadvantage of a crystalline form, at least in a

bulk configuration. Thus, the best candidates for replacing SiO_2 as a gate dielectric are those with high dielectric constant, a relatively large bandgap, and are able to be fabricated as a thin layer with an amorphous form.

Materials such as Ta_2O_3, TiO_2, Al_2O_3, HfO_2, $HfSi_xO_y$, $HfSi_xO_y$, and barium strontium titanate (BST) have been proposed as replacements for SiO_2 as gate dielectric materials. Additional materials have been proposed to not only provide a material layer with a dielectric constant greater than silicon dioxide, but also to provide adjustment to the insulating properties of the material. Such materials can be provided as nanolaminates, for example, Ta_2O_5/ HfO_2, ZrO_2/ HfO_2, Ta_2O_5/ HfO_2 nanolaminates. Providing dielectric layers configured as nanolaminates can provide a dielectric layer with relatively low leakage current properties.

In an embodiment of the present invention, a dielectric film having a chemical vapor deposited hafnium oxide and an electron beam evaporated lanthanide oxide allows for the engineering of a dielectric layer with a dielectric constant significantly higher than that of silicon dioxide and a relatively low leakage current characteristic. Using layers of chemical vapor deposited HfO_2 in various embodiments, provides layers, as compared to ZrO_2, that have a stronger tendency to form a single phase structure, a higher refractive index when deposited at low temperatures, a larger band gap, higher band offsets on silicon, and better thermal stability against silicide formation. Additionally, amorphous lanthanide oxides provide high oxide capacitance, low leakage current, and high thermal stability.

Another consideration for selecting materials for forming a dielectric layer concerns the roughness of the dielectric layer on a substrate. Surface roughness of the dielectric layer has a significant effect on the electrical properties of the gate oxide, and the resulting operating characteristics of the transistor. Leakage current through a physical 1.0 nanometer gate oxide has been found to be increased by a factor of 10 for every 0.1 increase in the root-mean-square (RMS) roughness.

During a conventional sputtering deposition process stage, particles of the material to be deposited bombard the surface at a high energy. When a particle hits the surface, some particles adhere, and other particles cause damage. High-energy

impacts remove body region particles creating pits. The surface of such a deposited layer may have a rough contour due to the rough interface at the body region.

Additionally, the localized non-flat surface morphology of CMOS devices, especially at edges of shallow trench isolations, may make a sputtering process a non-ideal process for CMOS fabrication. Further, a sputtering process introduces the possibility of a damaging effect to the channel region of CMOS devices. Using an alternate metalorganic chemical vapor deposition (MOCVD) process may introduce carbon contamination into a sensitive channel region of a CMOS device, since a MOCVD precursor contains carbon.

In an embodiment, a hafnium oxide layer is formed on a substrate by chemical vapor deposition using a precursor that does not contain carbon or other harmful elements. Further, a CVD precursor can be used that also does not contain chlorine or other halogens. A lanthanide oxide layer is then formed on the hafnium oxide layer, where the lanthanide oxide layer is formed by electron beam evaporation.

Figure 2 depicts a block diagram for an embodiment of a chemical vapor deposition system 200 for processing a layer of hafnium oxide for a dielectric layer containing a hafnium oxide and a lanthanide oxide. Commercial CVD systems are available that can be used for practicing embodiments of the present invention. Those of ordinary skill in the art of semiconductor fabrication understand the use, construction and fundamental operation of chemical vapor deposition chambers for deposition of material layers. Additionally, the elements of a CVD system such as system 200 may be controlled by a computer. To focus on the use of CVD system 200 in the various embodiments of the present invention, the computer is not shown in the block diagram of Figure 2.

Chemical vapor deposition system 200 includes a CVD reaction chamber 205 in which a substrate 210 is mounted in close proximity to a heater 215. Heater 215 is used to maintain substrate 210 at a given temperature during CVD processing. Heater 215 may be used according to various types and configurations of heaters, and arranged in a wide variety of orientations with respect to substrate 210 as are known to those skilled in the art. CVD system 200 also includes a source

220 for a hafnium containing precursor as well as for a carrier gas for the hafnium containing precursor. An additional source 230 provides oxygen gas with an associated carrier gas, such as argon.

Figure 3 depicts an electron beam evaporation system 300 for processing a layer of lanthanide oxide for a dielectric layer containing a hafnium oxide and a lanthanide oxide. Evaporation system 300 includes a reaction chamber 305 in which is located a substrate 310 having a surface 312 that is to be processed. Substrate 310 rests on substrate holder 315 and its temperature can be raised above room temperature using a heater 320 with its associated reflector 325. Evaporation system 300 also includes an electron gun device 330 regulated by electron gun controller 335 for depositing material on substrate surface 312.

Material evaporated using electron gun device 330 travels to substrate 310 through an ionizer ring 345 and shutter 350. Ionizer ring 345 provides supplemental oxygen for processes that require additional oxygen due to lost of oxygen in the evaporation of target materials. For target materials substantially void of oxygen, ionizer ring 345 provides initial oxygen to a film deposited on substrate surface 312 that is to undergo a subsequent oxidation process. Shutter 350 is used in conjunction with the control of electron gun device 330 to control the growth rate of a film on substrate 310. The growth rate is determined using quartz crystal monitors 355, 360. The quartz crystal monitors 355, 360 are coupled to a thickness/rate control 365, typically located outside reaction chamber 305.

Also located outside reaction chamber 305 is an oxygen gas source 370 including a mass-flow controller 375. In an embodiment, the oxygen gas source is ozone gas. Mass-flow controller 375 controls the flow of the oxygen source into reaction chamber 305. Further, a vacuum pump 380 with mass flow controller 385 maintains the overall atmosphere of evaporation system 300 at desired levels prior to, during, and after evaporation.

Electron gun device 330 can include an electron gun and receptacle for a target material that is to be evaporated. Target material placed in the target receptacle of electron gun device 330 is heated by impact from an electron beam from its associated electron gun. The electron beam is generated with an intensity

and duration with which to evaporate the material in the target receptacle of electron gun device 330. The evaporated material then distributes throughout the reaction chamber 305. The evaporated material and pre-evaporation contaminants are prevented from depositing on substrate surface 312 in an unwanted manner by

5   shutter 350. Further, electron gun device can be realized using commercially available devices as are known to those skilled in the art.

Ionizer ring 345 provides oxygen necessary to compensate for loss of oxygen in the evaporated target material, or to add initial oxygen for subsequent oxidation processing. In one embodiment, it includes a ring with a center axis. The

10   ring has a plurality of openings adapted to direct oxygen flowing to ionizer ring 345 from oxygen gas source 370 towards substrate surface 312. Oxygen is uniformly distributed to substrate surface 312 by ionizer ring 345 positioned generally parallel to substrate 310.

The electron beam evaporation chamber 300 can be included as part of an

15   overall processing system including CVD system 200 of Figure 2. To avoid contamination of the surface of a layer formed by chemical vapor deposition, evaporation chamber 300 can be connected to CVD system 200 using sealable connections to maintain the substrate, which is substrate 210 in Figure 2 and substrate 310 of Figure 3, in an appropriate environment between CVD processing

20   of a hafnium oxide layer and electron beam evaporation of a lanthanide oxide layer. Other means as are known to those skilled in the art can be employed for maintaining an appropriate environment between different processing procedures.

Figure 4 illustrates a flow diagram of elements for an embodiment of a method to process a dielectric layer containing a chemical vapor deposited hafnium

25   oxide layer and an electronic beam evaporated lanthanide oxide layer. This embodiment includes forming a layer of hafnium oxide by chemical vapor deposition, at block 410, and forming a layer of a lanthanide oxide by electron beam evaporation, at block 420, where the layer of hafnium oxide is adjacent to and in contact with the lanthanide oxide layer. The lanthanide oxide can be selected from

30   Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, and Dy_2O_3. In an embodiment the method includes forming the layer of hafnium oxide on a substrate and forming the layer of

lanthanide oxide on the layer of hafnium oxide. Alternately, a layer of lanthanide

oxide is formed on a substrate and a layer of hafnium oxide is formed on the layer

of lanthanide oxide. In an embodiment, the method includes controlling the forming

of the layer of hafnium oxide and the layer of the lanthanide oxide to form a

5   lanthanide oxide/hafnium oxide nanolaminate. The nanolaminate may have

multiple layers of different lanthanide oxides selected from Pr_2O_3, Nd_2O_3, Sm_2O_3,

Gd_2O_3, and Dy_2O_3.

For a dielectric layer having a hafnium oxide layer and one or more layers of

a lanthanide oxide, the combined thickness of lanthanide oxide layers can be limited

10   to a total thickness between about 2 nanometers and about 10 nanometers. Also,

for a dielectric layer having a lanthanide oxide layer and one or more layers of

hafnium oxide, the combined thickness of hafnium oxide layers can be limited to a

total thickness between about 2 nanometers and about 10 nanometers. In an

embodiment, hafnium oxide layers are limited to between about 2 nanometers and

15   about 5 nanometers. In an embodiment, a dielectric layer includes a hafnium oxide

layer and multiple layers of lanthanide oxide, where each layer of lanthanide oxide

is limited to a thickness between about 2 nanometers and about 10 nanometers.

Figure 5 illustrates a flow diagram of elements for an embodiment of a

method to process a dielectric layer containing a chemical vapor deposited hafnium

20   oxide layer and an electronic beam evaporated lanthanide oxide layer. In an

embodiment, the method depicted in Figure 5 can be used to form a gate dielectric

layer for a transistor. This embodiment may be implemented with the chemical

vapor deposition system 200 of Figure 2, and the electron beam evaporation system

of Figure 3.

25   At block 505, substrate 210 is prepared. Substrate 210 used for forming a

transistor is typically a silicon or silicon containing material. In other embodiments,

germanium, gallium arsenide, silicon-on-sapphire substrates, or other suitable

substrates may be used. This preparation process may include cleaning of substrate

210 and forming layers and regions of the substrate, such as drains and sources of a

30   metal oxide semiconductor (MOS) transistor, prior to forming a gate dielectric. In

an embodiment, the substrate is cleaned to provide an initial substrate depleted of its

native oxide. In an embodiment, the initial substrate is cleaned to provide a hydrogen-terminated surface. In an embodiment, a silicon substrate undergoes a final hydrofluoric acid, HF, rinse prior to CVD processing to provide the silicon substrate with a hydrogen-terminated surface without a native silicon oxide layer.

5   In an embodiment, substrate 210 is prepared as a chemical oxide-terminated silicon surface prior to forming a hafnium oxide by chemical vapor deposition. This preparation allows for forming an interface layer to provide a structure that may further aid in reducing the leakage current through the dielectric layer.

           The sequencing of the formation of the regions of the transistor being
10   processed follows typical sequencing that is generally performed in the fabrication of a MOS transistor as is well known to those skilled in the art. Included in the processing is the masking of substrate regions to be protected during the gate dielectric formation, as is typically performed in MOS fabrication. In this embodiment, the unmasked region may include a body region of a transistor;
15   however one skilled in the art will recognize that other semiconductor device structures may utilize this process. Additionally, substrate 210 in its ready for processing form is conveyed into a position in reaction chamber 205 for CVD processing.

           At block 510, a layer of hafnium oxide is formed by chemical vapor
20   deposition. In an embodiment, a sublimation technique is used for precursor delivery, where the precursor material is solid and held in source 220 and the substrate is maintained at a temperature ranging from about 200°C to about 400 °C. The sublimation temperature is maintained at about 63 °C with a vapor pressure of about 5 Torr. The precursor material is a hafnium-nitrato ($Hf(NO_3)_4$ precursor with
25   an argon carrier gas. Oxygen along with an argon carrier gas is provided from source 230. Alternately, the hafnium oxide layer can be formed without providing additional oxygen from source 230 with oxygen for the hafnium oxide provided by the decomposition of the $Hf(NO_3)_4$ precursor. Utilizing $Hf(NO_3)_4$ as the precursor for the chemical vapor deposition allows the use of only nitrogen and oxygen. As a
30   result, carbon is not introduced into the device being process during the formation of the hafnium oxide layer. Further, no halogen, such as chlorine, is introduced into

the device since a halide is not used. For embodiments in which the introduction of

carbon or halogen residue is not a significant detriment, other hafnium-containing

precursors, such as $C_{16}H_{36}HfO_4$, HfI_4, and $HfCl_4$, can be used in the CVD

processing of the hafnium oxide layer. Also, other CVD techniques may be used to

5   form the hafnium oxide layer.

Upon forming the CVD hafnium oxide layer, a determination is made as to

whether the desired number of layers of a lanthanide oxide has been formed, at

block 515. If the desired number of layers of a lanthanide oxide has been made, a

determination is made as to whether the desired number of layers of hafnium oxide

10   has been processed, at block 525. Such a case may occur in embodiments for a

dielectric layer having hafnium oxide formed as consecutive layers on a lanthanide

oxide layer. If more layers of hafnium oxide are required for the given application,

the overall process continues as a chemical vapor deposition, at block 510.

If it is determined, at block 515, that the desired number of layers of a

15   lanthanide oxide has not been formed, then a layer of lanthanide oxide is formed on

substrate 210, at block 520, which may include hafnium oxide layers and other

lanthanide oxide layers. Substrate 210 in the CVD system, as depicted in the block

diagram of Figure 2, is moved into the evaporation system depicted in Figure 3,

where the substrate 210, with its formed layers, becomes substrate 310 of Figure 3.

20   To avoid contamination of the surface of a layer formed by chemical vapor

deposition, evaporation chamber 300 can be connected to CVD system 200 using

sealable connections to maintain the substrate in an appropriate environment

between CVD processing of a hafnium oxide layer and electron beam evaporation

of a lanthanide oxide layer. Other means as are known to those skilled in the art can

25   be employed for maintaining an appropriate environment between different

processing procedures.

Substrate 310, suitably masked for the given application and process

procedures, is moved into evaporation chamber 305. Electron gun 330 contains a

receptacle for a source target on which an electron beam is directed. Electron gun

30   controller 335 regulates the rate of evaporation of material from the target source.

Alternatively, evaporation chamber 305 can include multiple electron guns, where

each electron gun is directed to different targets containing sources to form selected lanthanide oxides to be used at different times in the process.

In an embodiment, the target source of electron gun 330 contains a ceramic Pr_6O_{11} source, which is evaporated due to the impact of the electron beam. The evaporated material is then distributed throughout the chamber 305. A dielectric layer of Pr_2O_3 is grown on surface 312 of substrate 310, which is maintained at a temperature ranging from about 100 °C to about 150 °C. The growth rate can vary with a typical rate of 0.1 Å/s. In an embodiment in which a lanthanide is first formed on a substrate prior to forming a hafnium oxide layer, a Pr_2O_3 layer may include a thin amorphous interfacial layer separating a crystalline layer of Pr_2O_3 from the substrate on which it is grown. This thin amorphous layer may be beneficial in reducing the number of interface charges and eliminating any grain boundary paths for conductance from the substrate. Other source materials can be used for forming a Pr_2O_3 layer, as are known to those skilled in the art.

Alternately, the lanthanide oxide layer formed by electron beam evaporation for a dielectric layer containing a chemical vapor deposited hafnium oxide and a lanthanide oxide can be an oxide selected from Nd_2O_3, Sm_2O_3, Gd_2O_3, or Dy_2O_3. Further, a dielectric layer may include a number of hafnium oxide layers and a number of lanthanide oxide layers, where the lanthanide oxide layers are different lanthanide oxides. The different lanthanide oxides can be selected from Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, and Dy_2O_3. The source material for the particular lanthanide oxide is chosen from commercial materials for forming the lanthanide oxide by electron bean evaporation, as is known by those skilled in the art.

After forming the layer of lanthanide oxide, at block 520, a determination is made as to whether the desired number of hafnium oxide layers has been formed, at block 525. If the desired number of hafnium oxide layers has not been formed, substrate 310 is moved back into chemical vapor deposition system 200 and the process continues, at block 510. If it is determined that the desired number of hafnium oxide layers have been formed, at block 525, it is then determined whether the desired number of layers of a lanthanide oxide have been formed, at block 530. If the desired number of lanthanide oxide layers has not been formed, a layer of

lanthanide oxide is formed by electron beam evaporation, at block 520, and the process continues. If is determined that the desired number of lanthanide oxide layers has been formed, at block 530, and if the desired number of hafnium oxide layers has been formed, then the substrate is further processed to complete device

5   processing, at block 535.

If the dielectric layer containing a chemical vapor deposited hafnium oxide and an electron beam evaporated lanthanide oxide has been formed to have the desired thickness, the growth of the dielectric layer is complete. The dielectric layer may be annealed. To avoid the diffusion of oxygen during annealing to the

10   semiconductor substrate surface, annealing may be performed in an oxygen-free environment for short periods of time. An embodiment of an annealing environment may include a nitrogen atmosphere. In addition to limiting or avoiding oxygen diffusion to the semiconductor substrate, the relatively low processing temperatures employed by chemical vapor deposition of the hafnium oxide layers

15   and by electron beam evaporation of the lanthanide layers allows for the formation of an amorphous dielectric layer.

At block 535, after forming the dielectric film containing chemical vapor deposited hafnium oxide and electron beam deposited lanthanide oxide, processing the device having this dielectric layer is completed. In an embodiment, completing

20   the device includes completing the formation of a transistor. In an embodiment, completing the device includes completing the formation of a capacitor. In an embodiment, completing the process includes completing the construction of a memory device having an array with access transistors formed with gate dielectrics containing chemical vapor deposited hafnium oxide and electron beam deposited

25   lanthanide oxide. In an embodiment, completing the process includes the formation of an electronic system including an information handling device that uses electronic devices with transistors formed with dielectric layers having a chemical vapor deposited hafnium oxide and an electron beam deposited lanthanide oxide.

Upon reading and comprehending this disclosure, it can be appreciated by

30   those skilled in the art that the elements of a method for forming a dielectric layer containing chemical vapor deposited hafnium oxide and electron beam deposited

lanthanide oxide in the embodiment of Figure 5 may be performed under various environmental conditions, including various pressures and temperatures, for a given application and the systems used to fabricate such a dielectric layer. Determination of the environmental conditions, precursors used, and electron beam target materials

5   may be made without undue experimentation.

The elements for a method for forming a dielectric layer containing a chemical vapor deposited hafnium oxide and an electron beam deposited lanthanide oxide as illustrated in Figure 5 can vary and include numerous permutations. In an embodiment, a chemical vapor deposited hafnium oxide layer is formed on a

10   substrate and an electron beam evaporated lanthanide oxide layer is formed on the hafnium oxide layer. Alternately, an electron beam evaporated lanthanide oxide layer is formed on a substrate and a chemical vapor deposited hafnium oxide layer is deposited on the lanthanide oxide layer. A hafnium oxide layer may be formed as multiple layers of chemical vapor deposited hafnium oxide. Similarly, a lanthanide

15   oxide layer may be formed as multiple layers of an electron beam evaporated lanthanide oxide. Additionally, a dielectric layer may contain multiple layers of lanthanide oxide, where two or more layers contain different lanthanide oxides selected from Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, and Dy_2O_3.

In an embodiment, a dielectric containing a chemical vapor deposited

20   hafnium oxide and an electron beam evaporated lanthanide oxide is formed as a nanolaminate. The nanolaminate may have multiple layers of different lanthanide oxides selected from Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, and Dy_2O_3. For a dielectric layer having a hafnium oxide layer and one or more layers of a lanthanide oxide, the combined thickness of lanthanide oxide layers can range from about 2 nanometers

25   to about 10 nanometers. Also, for a dielectric layer having a lanthanide oxide layer and one or more layers of hafnium oxide, the combined thickness of hafnium oxide layers can range from about 2 nanometers to about 10 nanometers. In an embodiment, the combined thickness of the hafnium oxide layers ranges from about 2 nanometers to about 5 nanometers. In an embodiment, a dielectric layer includes

30   a hafnium oxide layer and multiple layers of lanthanide oxide, where each layer of lanthanide oxide has a thickness ranging from about 2 nanometers to about 10

nanometers. In an embodiment, a dielectric layer includes a lanthanide oxide layer and multiple layers of hafnium oxide, where each layer of hafnium oxide has a thickness ranging from about 2 nanometers to about 10 nanometers. In an embodiment, a dielectric layer containing a chemical vapor deposited hafnium oxide layer and an electron beam evaporated lanthanide oxide layer has a thickness ranging from about 2 nanometers to about 20 nanometers.

A dielectric layer containing a chemical vapor deposited hafnium oxide and an electron beam deposited lanthanide oxide may be processed in a chemical vapor deposition system such as CVD system 200 and evaporation system 300 under computer control. Instructions stored in a computer readable medium are executed by a computer to accurately control the integrated functioning of the elements of chemical vapor deposition system 200 and evaporation system 300 to form a dielectric layer containing hafnium oxide and a lanthanide oxide, according to various embodiments. The computer-executable instructions may be provided in any computer-readable medium. Such computer-readable medium may include, but is not limited to, floppy disks, diskettes, hard disks, CD-ROMS, flash ROMS, nonvolatile ROM, and RAM.

Dielectric layers containing chemical vapor deposited hafnium oxide layers and electron beam evaporated lanthanide oxide layers can have a wide range of dielectric constants determined by the series configuration and relative thickness of the hafnium oxide layers and the lanthanide oxide layers. In bulk form, HfO_2 has a dielectric constant of about 25. Bulk Pr_2O_3 has a dielectric constant of about 31, while the dielectric constants for Nd_2O_3, Sm_2O_3, Gd_2O_3, and Dy_2O_3, in bulk form, are generally also in the range of 25-30. Consequently, a dielectric layer containing bulk layers of hafnium oxide and lanthanide oxide could be expected to have a dielectric constant engineered in the range from about 25 to about 31. Such a dielectric layer would have a t_{eq} that is about one-sixth to one-eight smaller than a silicon oxide layer of the same thickness.

However, a thin dielectric layer with an interfacial layer formed between the surface of the substrate and the first layer of a hafnium oxide or a lanthanide oxide will have a t_{eq} that is based on an interfacial layer physically in parallel with the

dielectric layer equivalently forming a series configuration of electrical structures. Thus, the dielectric layer formed having an interfacial layer between it and the substrate on which it is grown can have an effective dielectric constant considerably less than a dielectric constant associated with the combination of hafnium oxide and

5   lanthanide oxide layers.

Effective dielectric constants associated with thin layers of Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, and Dy_2O_3 oxides on silicon have been reported to have dielectric constants in the range of 11 to 15 with interfacial regions having a thickness in the of about 0.5 nm to about 1.1 nm. *See J. Sanghun et al., Technical Digest of*

10   *International Electron Devices Meetings 2001, pp. 471-474 (2001).* Similarly, chemical vapor deposited HfO_2 also has been reported to have an effective dielectric constant reduced from its bulk value to a value in the range of 18 to 22 when formed as a thin layer on a silicon substrate with an interfacial layer. *See J. Park et al., Journal of the Electrochemical Society, vol. 149: no. 1, pp. G89-G94 (2002).* The

15   effective dielectric constants for thin dielectric layers containing any of these materials and/or combinations of these materials may be reduced from their bulk value depending on the thickness and material composition of any interfacial layer that may be formed.

Further, for those cases in which a dielectric layer containing chemical vapor

20   deposited hafnium oxide and electron beam evaporated lanthanide oxide is formed with little or no interfacial layer, the dielectric layer may be subject to a thin film effect related to the abrupt termination of the film. A planar bulk or thick film can be considered as a bulk region with two surface regions. Due to the termination of the thick film, the properties of the two surface regions can vary from that of the

25   bulk region. In a thick film, the effective properties of the film are dominated by the bulk region. In a thin film, including nanolaminates, the properties of the thin film are effectively controlled by two surface regions. *See K. Natori et al., Applied Physics Letters, vol. 73: no. 5, pp. 632-634 (1998).* Thus, thin films of hafnium oxide and lanthanide oxide may have effective dielectric constants reduced from

30   their bulk values without being formed in a structure with interfacial regions. Without a size effect, dielectric layers containing hafnium oxide and lanthanide

oxide may have a dielectric constant in the range of about 25 to about 31. With a

size effect, dielectric layers containing hafnium oxide and lanthanide oxide may

have dielectric constants in the range from about 11 to about 16.

The embodiments described herein provide a process for growing a

5 dielectric layer containing a chemical vapor deposited hafnium oxide and an

electron beam evaporated lanthanide oxide having a wide range of useful equivalent

oxide thickness, t_{eq}. The relatively large dielectric constant for such a dielectric

layer ranges from about 11 to about 31, depending on the presence of an interfacial

layer and/or on a size effect. Forming a dielectric layer according to various

10 embodiments with a thickness ranging from 2 nanometers to 20 nanometers allows

for the engineering of dielectric layers achieving a t_{eq} in the range of about .7

nanometers to about 7 nanometers. Without an interfacial layer and without a size

effect, the t_{eq} for such a dielectric layer may range from about .25 nanometers to

about 2.5 nanometers. A dielectric layer containing a chemical vapor deposited

15 hafnium oxide and an electron beam evaporated lanthanide oxide may be formed for

applications with a t_{eq} between 10Å and 20Å, or less than 10Å.

Dielectric layers containing a chemical vapor deposited hafnium oxide and

an electron beam evaporated lanthanide oxide using embodiments of the present

invention may be engineered with various structures and compositions including an

20 amorphous structure. Embodiments using low processing temperatures tend to

provide an amorphous structure, which is better suited for reducing leakage current

than structures exhibiting a polycrystalline structure or a partial polycrystalline

structure.

Figure 6 depicts a nanolaminate structure 600 for an embodiment of a

25 dielectric structure including chemical vapor deposited hafnium oxide and electron

beam evaporated lanthanide oxide. Nanolaminate structure 600 includes a plurality

of layers 605-1 to 605-N, where each layer contains chemical vapor deposited

hafnium oxide or electron beam evaporated lanthanide oxide. The sequencing of

the layers depends on the application. The effective dielectric constant associated

30 with nanolaminate structure 600 is that attributable to N capacitors in series, where

each capacitor has a thickness defined by the thickness of the corresponding

electron beam evaporated lanthanide oxide or chemical vapor deposited hafnium oxide layer. By selecting each thickness and the composition of each layer, electron beam evaporated lanthanide oxide or chemical vapor deposited hafnium oxide layer, a nanolaminate structure can be engineered to have a predetermined dielectric

5   constant.

Embodiments for forming a dielectric layer including CVD processing of a hafnium oxide and processing of an lanthanide oxide by electron beam evaporation may be implemented to form transistors, capacitors, memory devices, and other electronic systems including electro-optic devices, microwave devices, and

10   information handling devices. With careful preparation and engineering of the dielectric layer limiting the size of interfacial regions, a t_{eq} less than about 10 Å for these devices is anticipated.

A transistor 100 as depicted in Figure 1 may be constructed by forming a source region 120 and a drain region 130 in a silicon based substrate 110 where

15   source and drain regions 120, 130 are separated by a body region 132. Body region 132 defines a channel having a channel length 134. A dielectric layer is disposed on substrate 110 formed as a layer containing a chemical vapor deposited hafnium oxide and an electron beam evaporated lanthanide oxide. The resulting dielectric layer forms gate dielectric 140.

20   A gate 150 is formed over gate dielectric 140. Typically, forming gate 150 may include forming a polysilicon layer, though a metal gate may be formed in an alternative process. An interfacial layer 133 may form between body region 132 and gate dielectric 140. In an embodiment, interfacial layer 133 may be limited to a relatively small thickness compared to gate dielectric 140, or to a thickness

25   significantly less than gate dielectric 140 as to be effectively eliminated. Forming the substrate, the source and drain regions, and the gate is performed using standard processes known to those skilled in the art. Additionally, the sequencing of the various elements of the process for forming a transistor is conducted with standard fabrication processes, also as known to those skilled in the art.

30   The method for forming a dielectric layer containing a chemical vapor deposited hafnium oxide and an electron beam evaporated lanthanide oxide in

various embodiments may be applied to other transistor structures having dielectric layers. Figure 7 shows an embodiment of a configuration of a transistor 700 having a dielectric layer containing a chemical vapor deposited hafnium oxide and an electron beam evaporated lanthanide oxide. Transistor 700 includes a silicon based

5   substrate 710 with a source 720 and a drain 730 separated by a body region 732. Body region 732 between source 720 and drain 730 defines a channel region having a channel length 734. Located above body region 732 is a stack 755 including a gate dielectric 740, a floating gate 752, a floating gate dielectric 742, and a control gate 750. Gate dielectric 740 includes a dielectric containing a chemical vapor

10   deposited hafnium oxide layer and an electron beam evaporated lanthanide oxide layer as described herein with the remaining elements of the transistor 700 formed using processes known to those skilled in the art. Alternately, both gate dielectric 740 and floating gate dielectric 742 may be formed as dielectric layers containing a chemical vapor deposited hafnium oxide and an electron beam evaporated

15   lanthanide oxide in various embodiments as described herein. An interfacial layer 733 may form between body region 732 and gate dielectric 740. In an embodiment, interfacial layer 733 may be limited to a relatively small thickness compared to gate dielectric 740, or to a thickness significantly less than gate dielectric 740 as to be effectively eliminated.

20   The embodiments of methods for forming dielectric layers containing a chemical vapor deposited hafnium oxide and an electron beam evaporated lanthanide oxide may also be applied to forming capacitors in various integrated circuits, memory devices, and electronic systems. In an embodiment for forming a capacitor 800 illustrated in Figure 8, a method includes forming a first conductive

25   layer 810, forming a dielectric layer 820 containing a chemical vapor deposited hafnium oxide and an electron beam evaporated lanthanide oxide on first conductive layer 810, and forming a second conductive layer 830 on dielectric layer 820. An interfacial layer 815 may form between first conductive layer 810 and dielectric layer 820. In an embodiment, interfacial layer 815 may be limited to a relatively

30   small thickness compared to dielectric layer 820, or to a thickness significantly less than dielectric layer 820 as to be effectively eliminated.

Transistors, capacitors, and other devices dielectric layers containing a
chemical vapor deposited hafnium oxide and an electron beam evaporated
lanthanide oxide using methods described herein may be implemented into memory
devices and electronic systems including information handling devices. Such

5   information devices may include wireless systems, telecommunication systems, and
computers. It will be recognized by one skilled in the art that several types of
memory devices and electronic systems including information handling devices
utilize embodiments of the present invention.

Figure 9 is a simplified block diagram of a memory device 900 using an
10   embodiment of a dielectric containing a chemical vapor deposited hafnium oxide
and an electron beam evaporated lanthanide oxide. Memory device 900 includes an
array of memory cells 902, address decoder 904, row access circuitry 906, column
access circuitry 908, control circuitry 910, and Input/Output (I/O) circuit 912. The
memory is operably coupled to an external microprocessor 914, or memory
15   controller for memory accessing. Memory device 900 receives control signals from
processor 914, such as WE*, RAS* and CAS* signals, which can be supplied on a
system bus. Memory device 900 stores data that is accessed via I/O lines. Each
memory cell in a row of memory cell array 902 is coupled to a common word line.
The word line is coupled to gates of individual transistors, where at least one
20   transistor has a gate coupled to a gate dielectric containing a chemical vapor
deposited hafnium oxide and an electron beam evaporated lanthanide oxide in
accordance with the methods and structure previously described herein.
Additionally, each memory cell in a column is coupled to a common bit line. Each
cell in memory array 902 may include a storage capacitor and an access transistor as
25   is conventional in the art. It will be appreciated by those skilled in the art that
additional circuitry and control signals can be provided, and that the memory device
of Figure 9 has been simplified to focus on embodiments of the present invention.

It will be understood that the above description of a memory device is
intended to provide a general understanding of the memory and is not a complete
30   description of all the elements and features of a specific type of memory, such as
DRAM (Dynamic Random Access Memory). Further, embodiments are equally

applicable to any size and type of memory circuit and are not intended to be limited to the DRAM described above. Other alternative types of devices include SRAM (Static Random Access Memory) or Flash memories. Additionally, the DRAM could be a synchronous DRAM commonly referred to as SGRAM (Synchronous

5   Graphics Random Access Memory), SDRAM (Synchronous Dynamic Random Access Memory), SDRAM II, and DDR SDRAM (Double Data Rate SDRAM), as well as Synchlink or Rambus DRAMs and other emerging DRAM technologies.

Figure 10 illustrates a block diagram for an electronic system 1000 having devices with an embodiment for a dielectric layer containing a chemical vapor

10   deposited hafnium oxide and an electron beam evaporated lanthanide oxide. Electronic system 1000 includes a controller 1005, a bus 1015, and an electronic device 1025, where bus 1015 provides electrical conductivity between controller 1005 and electronic device 1025. In various embodiments, controller 1005 and/or electronic device 1025 include an embodiment for a dielectric layer containing a

15   chemical vapor deposited hafnium oxide and an electron beam evaporated lanthanide oxide as previously discussed herein. In an embodiment, electronic system 1000 includes a plurality of electronic devices using an embodiment for a dielectric layer containing a chemical vapor deposited hafnium oxide and an electron beam evaporated lanthanide oxide according to the present invention.

20   Electronic system 1000 may include, but is not limited to, information handling devices, wireless systems, telecommunication systems, fiber optic systems, electro-optic systems, and computers.

Conclusion

25   A dielectric layer containing a chemical vapor deposited hafnium oxide and an electron beam evaporated lanthanide oxide, using methods described herein, provides a reliable dielectric layer having an equivalent oxide thickness thinner than attainable using SiO_2. The formation of these dielectric layers provides for enhanced dielectric and electrical properties relative to those attained with an

30   amorphous SiO_2 layer. Additionally, forming hafnium oxide layers by chemical vapor deposition with precursors not containing carbon permits the formation of the

hafnium oxide layers without unwanted contamination associated with carbon residue. These properties of dielectric layers containing a chemical vapor deposited hafnium oxide and an electron beam evaporated lanthanide oxide allow for application as dielectric layers in numerous devices and systems.

5   Capacitors, transistors, electro-optic devices, higher level ICs or devices, and electronic systems are constructed utilizing various embodiments for forming a dielectric layer containing a chemical vapor deposited hafnium oxide and an electron beam evaporated lanthanide oxide structured to provide an ultra thin equivalent oxide thickness, t_{eq}. Dielectric layers containing a chemical vapor

10   deposited hafnium oxide and an electron beam evaporated lanthanide oxide are formed having a dielectric constant substantially higher than that of silicon dioxide, where such dielectric layers are capable of a t_{eq} thinner than 10 Å, thinner than the expected limit for SiO_2 gate dielectrics. The thinner t_{eq} of these dielectric layers allows for a higher capacitance than SiO_2 gate dielectrics, which provides further

15   effective scaling for microelectronic devices and systems. At the same time, the physical thickness of the dielectric layer containing a chemical vapor deposited hafnium oxide and an electron beam evaporated lanthanide oxide is much larger than the SiO_2 thickness associated with the t_{eq} limit of SiO_2. Forming the larger thickness aids in the manufacturing process for dielectric layers.

20   Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. This application is intended to cover any adaptations or variations of the present invention. It is to be understood that the above description

25   is intended to be illustrative, and not restrictive. Combinations of the above embodiments, and other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the present invention includes any other applications in which the above structures and fabrication methods are used. The scope of the present invention should be determined with reference to the

30   appended claims, along with the full scope of equivalents to which such claims are entitled.